Amendments to the claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claims 1-13 (canceled)

Claim 14 (currently amended): A method for picture-in-picture insertion,

wherein a sequence of insertion pictures ~~(Kj=K1,K2,...)~~ decimated by vertical decimation ~~(VD ≥ 1)~~ are read into a memory device ~~(S)~~ and subsequently read out,

wherein the insertion pictures ~~(Kj)~~ read out are inserted into a sequence of main pictures ~~(Hi=H1, H2,...)~~,

wherein the memory device ~~(S)~~ has a storage capacity of greater than one insertion picture but less than two insertion pictures ~~(Kj)~~ and is subdivided into memory segments ~~(X,Y,Z;A,B,C,D,E)~~ which are continuously overwritten by the insertion pictures, and

wherein a decision is made as to whether the currently written insertion picture ~~(Kj)~~ or the immediately preceding insertion picture ~~(Kj-1)~~ is read out,

wherein more than one memory segment ~~(X,Y,Z;A,B,C,D,E)~~ of the memory device ~~(S)~~ is required for storing an insertion picture ~~(Kj)~~, and in that the memory segments ~~(X,Y,Z;A,B,C,D,E)~~ of the memory device ~~(S)~~ are cyclically overwritten by the insertion pictures ~~(Kj)~~ in a predetermined order.

Claim 15 (currently amended): The method of claim 14 wherein the memory segments ~~(X,Y,Z;A,B,C,D,E)~~ are the same size.

Claim 16 (currently amended): The method of claim 14 wherein in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area ~~(I,II; I,II,III)~~ holding the currently written insertion

picture, a decision is made as to whether the currently written insertion picture ~~(Kj)~~ or the immediately preceding insertion picture ~~(Kj-1)~~ is read out.

Claim 17 (previously presented): The method of claim 14 wherein the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

Claim 18 (previously presented): The method of claim 17 wherein the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

Claim 19 (currently amended): The method of claim 18 wherein a memory segment has a storage capacity of 1/VD times the storage capacity required for an insertion picture and the decision criterion that is applied is whether the last memory segment ~~(H; III)~~ required for the currently written insertion picture is already being written too.

Claim 20 (previously presented): The method of claim 14 wherein the insertion pictures (Kj) and main pictures (Hi) are fields of a monitor picture.

Claim 21 (currently amended): The method of claim 14 wherein a comparison is made to determine whether a main picture ~~(Hi)~~ and an insertion picture ~~(Ki)~~ to be inserted into the latter have an identical field position, and, in the case of a differing field position, an identical field position is achieved by address shifting of the main picture ~~(Hi)~~ or of the insertion picture.

Claim 22 (currently amended): A circuit arrangement for picture-in-picture insertion, comprising: ~~having~~

a memory device ~~(S)~~ for storing vertically decimated insertion pictures ~~(Kj=K1, K2,...)~~, the memory device ~~(S)~~ having a storage capacity of greater than one insertion picture but less than two insertion pictures ~~(Kj)~~ and being subdivided into memory segments ~~(X,Y,Z;A,B,C,D,E)~~ which can be continuously overwritten by the insertion pictures; ~~(Kj), having~~

a control device ~~(3)~~ for reading out the vertically decimated insertion pictures from the memory device ~~(S)~~ and for inserting the insertion pictures ~~(Kj)~~ read out into a sequence of main pictures; ~~(Hi=H1, H2..),~~ and

~~having~~ a decision device for deciding whether the currently written insertion picture ~~(Kj)~~ or the immediately preceding insertion picture ~~(Kj-1)~~ is read out,

wherein each memory segment ~~(X,Y,Z;A,B,C,D,E)~~ has a storage capacity of less than one insertion picture ~~(Kj)~~, and

~~in that~~ the memory segments ~~(X,Y,Z;A,B,C,D,E)~~ of the memory device ~~(S)~~ can be cyclically overwritten by the insertion pictures ~~(Kj)~~ in a predetermined order.

Claim 23 (currently amended): The circuit arrangement of claim 22 wherein the memory segments ~~(X,Y,Z;A,B,C,D,E)~~ are the same size.

Claim 24 (previously presented): The circuit arrangement of claim 22 wherein the memory device has a storage capacity which is (2-1/VD) times the storage capacity required for an insertion picture, where VD is the vertical decimation of the insertion picture.

Claim 25 (previously presented): The circuit arrangement of claim 24 wherein the memory segments are the same size and the number of memory segments is 2* VD-1, the number of memory segments required for an insertion picture corresponding to the vertical decimation (VD).

Claim 26 (currently amended): The circuit arrangement of claim 22 wherein in a manner dependent on the ratio of a reading speed of a read pointer to a writing speed of a write pointer and a relative position of the write pointer in a writing area holding the currently written insertion picture, the decision device decides whether the currently written insertion picture ~~(Kj)~~ or the immediately preceding insertion picture ~~(Kj-1)~~ is read out.